PCT

REQUEST

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty.

For Receiving Office use only

International Application No.

International Filing Date

Name of receiving Office and "PCT International Application"

Applicant's or agent's file reference (If desired) (12 characters maximum) WOP12926A

Box No. I TITLE OF INVENTION

Semiconductor Device Simulation Method and Simulator

Box No. II APPLICANT

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

Seiko Epson Corporation
4-1, Nishishinjuku 2-chome, Sinjuku-ku,
Tokyo 163-0811
Japan

☐ This person is also inventor.

Telephone No.

Facsimile No.

Teleprinter No.

State *(that is, country)* of nationality: JP

State *(that is, country)* of residence: JP

This person is applicant for the purposes of: ☐ all designated States ☒ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

LUI Basil
Epson Cambridge Laboratory
8c Kings Parade
Cambridge CB2 1SJ
GB

This person is:
☐ applicant only
☒ applicant and inventor
☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality: GB

State *(that is, country)* of residence: GB

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☒ the United States of America only ☐ the States indicated in the Supplemental Box

☐ Further applicants and/or (further) inventors are indicated on a continuation sheet.

Box No. IV AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as: ☒ agent ☐ common representative

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

STURT Clifford Mark
Miller Sturt Kenyon
9 John Street
London WC1N 2ES
GB

Telephone No. +44(0)20 7242 5974

Facsimile No. +44(0)20 7430 0275

Teleprinter No.

☐ **Address for correspondence:** Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.

Box V DESIGNATION OF STATES

The following designations are hereby made under Rule 4.9(a) *(mark the applicable check-boxes; at least one must be marked)*:

Regional Patent

- ☒ AP ARIPO Patent: GH Ghana, GM Gambia, KE Kenya, LS Lesotho, MW Malawi, SD Sudan, SL Sierra Leone, SZ Swaziland, TZ United Republic of Tanzania, UG Uganda, ZW Zimbabwe, and any other State which is a Contracting State of the Harare Protocol and of the PCT
- ☒ EA Eurasian Patent: AM Armenia, AZ Azerbaijan, BY Belarus, KG Kyrgyzstan, KZ Kazakhstan, MD Republic of Moldova, RU Russian Federation, TJ Tajikistan, TM Turkmenistan, and any other State which is a Contracting State of the Eurasian Patent Convention and of the PCT
- ☒ EP European Patent: AT Austria, BE Belgium, CH and LI Switzerland and Liechtenstein, CY Cyprus, DE Germany, DK Denmark, ES Spain, FI Finland, FR France, GB United Kingdom, GR Greece, IE Ireland, IT Italy, LU Luxembourg, MC Monaco, NL Netherlands, PT Portugal, SE Sweden, and any other State which is a Contracting State of the European Patent Convention and of the PCT
- ☒ OA OAPI Patent: BF Burkina Faso, BJ Benin, CF Central African Republic, CG Congo, CI Côte d'Ivoire, CM Cameroon, GA Gabon, GN Guinea, GW Guinea-Bissau, ML Mali, MR Mauritania, NE Niger, SN Senegal, TD Chad, TG Togo, and any other State which is a member State of OAPI and a Contracting State of the PCT *(if other kind of protection or treatment desired, specify on dotted line)* .....

National Patent *(if other kind of protection or treatment desired, specify on dotted line)*:

- ☒ AE United Arab Emirates
- ☒ AL Albania
- ☒ AM Armenia
- ☒ AT Austria
- ☒ AU Australia
- ☒ AZ Azerbaijan
- ☒ BA Bosnia and Herzegovina
- ☒ BB Barbados
- ☒ BG Bulgaria
- ☒ BR Brazil
- ☒ BY Belarus
- ☒ CA Canada
- ☒ CH and LI Switzerland and Liechtenstein
- ☒ CN China
- ☒ CR Costa Rica
- ☒ CU Cuba
- ☒ CZ Czech Republic
- ☒ DE Germany
- ☒ DK Denmark
- ☒ DM Dominica
- ☒ EE Estonia
- ☒ ES Spain
- ☒ FI Finland
- ☒ GB United Kingdom
- ☒ GD Grenada
- ☒ GE Georgia
- ☒ GH Ghana
- ☒ GM Gambia
- ☒ HR Croatia
- ☒ HU Hungary
- ☒ ID Indonesia
- ☒ IL Israel
- ☒ IN India
- ☒ IS Iceland
- ☒ JP Japan
- ☒ KE Kenya
- ☒ KG Kyrgyzstan
- ☒ KP Democratic People's Republic of Korea
- ☒ KR Republic of Korea
- ☒ KZ Kazakhstan
- ☒ LC Saint Lucia
- ☒ LK Sri Lanka
- ☒ LR Liberia
- ☒ LS Lesotho
- ☒ LT Lithuania
- ☒ LU Luxembourg
- ☒ LV Latvia
- ☒ MA Morocco
- ☒ MD Republic of Moldova
- ☒ MG Madagascar
- ☒ MK The former Yugoslav Republic of Macedonia
- ☒ MN Mongolia
- ☒ MW Malawi
- ☒ MX Mexico
- ☒ NO Norway
- ☒ NZ New Zealand
- ☒ PL Poland
- ☒ PT Portugal
- ☒ RO Romania
- ☒ RU Russian Federation
- ☒ SD Sudan
- ☒ SE Sweden
- ☒ SG Singapore
- ☒ SI Slovenia
- ☒ SK Slovakia
- ☒ SL Sierra Leone
- ☒ TJ Tajikistan
- ☒ TM Turkmenistan
- ☒ TR Turkey
- ☒ TT Trinidad and Tobago
- ☒ TZ United Republic of Tanzania
- ☒ UA Ukraine
- ☒ UG Uganda
- ☒ US United States of America
- ☒ UZ Uzbekistan
- ☒ VN Viet Nam
- ☒ YU Yugoslavia
- ☒ ZA South Africa
- ☒ ZW Zimbabwe

Check-boxes reserved for designating States which have become party to the PCT after issuance of this sheet:

- ☐ .....
- ☐ .....

Precautionary Designation Statement: In addition to the designations made above, the applicant also makes under Rule 4.9(b) all other designations which would be permitted under the PCT except any designation(s) indicated in the Supplemental Box as being excluded from the scope of this statement. The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit. *(Confirmation (including fees) must reach the receiving Office within the 15-month time limit.)*

See Notes to the request form

Sheet No. .....

Box ... VI PRIORITY ... M ☐ Further priority ... are indicated in the Supplemental Box.

Filing date of earlier application (day/month/year)	Number of earlier application	Where earlier application is: national application: country	regional application:* regional Office	international application: receiving Office
item (1) 15 June 1999 15/06/99	9913915.6	GB		
item (2)				
item (3)				

☒ The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) *(only if the earlier application was filed with the Office which for the purposes of the present international application is the receiving Office)* identified above as item(s): (1)

* *Where the earlier application is an ARIPO application, it is mandatory to indicate in the Supplemental Box at least one country party to the Paris Convention for the Protection of Industrial Property for which that earlier application was filed (Rule 4.10(b)(ii)). See Supplemental Box.*

Box No. VII INTERNATIONAL SEARCHING AUTHORITY

Choice of International Searching Authority (ISA) *(if two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used)*: ISA/ EP

Request to use results of earlier search; reference to that search *(if an earlier search has been carried out by or requested from the International Searching Authority)*: Date *(day/month/year)* Number Country *(or regional Office)*

Box No. VIII CHECK LIST; LANGUAGE OF FILING

This international application contains the following number of sheets:

request	:	3
description (excluding sequence listing part)	:	8
claims	:	3
abstract	:	1
drawings	:	8
sequence listing part of description	:	
Total number of sheets	:	23

This international application is accompanied by the item(s) marked below:

1. ☒ fee calculation sheet
2. ☐ separate signed power of attorney
3. ☐ copy of general power of attorney; reference number, if any:
4. ☐ statement explaining lack of signature
5. ☐ priority document(s) identified in Box No. VI as item(s):
6. ☐ translation of international application into (language):
7. ☐ separate indications concerning deposited microorganism or other biological material
8. ☐ nucleotide and/or amino acid sequence listing in computer readable form
9. ☐ other *(specify)*:

Figure of the drawings which should accompany the abstract:

Language of filing of the international application: ENGLISH

Box No. IX SIGNATURE OF APPLICANT OR AGENT

Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the request).

Clifford M Sturt
Representative

For receiving Office use only

1. Date of actual receipt of the purported international application:
3. Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application:
4. Date of timely receipt of the required corrections under PCT Article 11(2):
5. International Searching Authority (if two or more are competent): ISA/
6. ☐ Transmittal of search copy delayed until search fee is paid.

2. Drawings:
☐ received:
☐ not received:

For International Bureau use only

Date of receipt of the record copy by the International Bureau:

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
WOP12926A		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/GB 00/ 02321	15/06/2000	15/06/1999
Applicant		
SEIKO EPSON CORPORATION		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 2 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. –

   [ ] as suggested by the applicant.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [X] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
GB 00/02321

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F17/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	LUI O K B ET AL: "A new generation-recombination model for device simulation including the Poole-Frenkel effect and phonon-assisted tunnelling" SOLID STATE ELECTRONICS,GB,ELSEVIER SCIENCE PUBLISHERS, BARKING, vol. 41, no. 4, 1 April 1997 (1997-04-01), pages 575-583, XP004056839 ISSN: 0038-1101 cited in the application the whole document	1-8

☐ Further documents are listed in the continuation of box C.

☐ Patent family members are listed in annex.

° Special categories of cited documents :

'A' document defining the general state of the art which is not considered to be of particular relevance

'E' earlier document but published on or after the international filing date

'L' document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

'O' document referring to an oral disclosure, use, exhibition or other means

'P' document published prior to the international filing date but later than the priority date claimed

'T' later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

'X' document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

'Y' document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

'&' document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 December 2000	28/12/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Guingale, A

Form PCT/ISA/210 (second sheet) (July 1992)

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 December 2000 (21.12.2000)

PCT

(10) International Publication Number
WO 00/77533 A2

(51) International Patent Classification[7]: G01R 31/00

(21) International Application Number: PCT/GB00/02321

(22) International Filing Date: 15 June 2000 (15.06.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
9913915.6 15 June 1999 (15.06.1999) GB

(71) Applicant *(for all designated States except US)*: **SEIKO EPSON CORPORATION** [JP/JP]; 4-1, Nishishinjuku 2-chome, Shinjuku-ku, Tokyo 163-0811 (JP).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **LUI, Basil** [GB/GB]; Epson Cambridge Laboratory, 8c Kings Parade, Cambridge CB2 1SJ (GB).

(74) Agent: **STURT, Clifford, Mark**; Miller Sturt Kenyon, 9 John Street, London WC1N 2ES (GB).

(81) Designated States *(national)*: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *Without international search report and to be republished upon receipt of that report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SEMICONDUCTOR DEVICE SIMULATION METHOD AND SIMULATOR

(57) Abstract: An automated simulation method for determining the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral and to a simulator for carrying out the method are disclosed. The method and simulator are, for example, particularly useful in the modelling of characteristics such as leakage current in polysilicon TFTs, which leakage current can, for example, seriously degrade pixel voltage in active matrix display devices. The simulator embodies the method, which method comprises the steps of: assigning the variable C to the ratio of the Poole-Frenkel barrier lowering energy (ΔE_{fp}) divided by the energy range for which tunnelling can occur (ΔE_n); assigning the value (C+1)/2 to a variable v and performing a second order Taylor's series expansion of the Dirac coulombic tunnelling integral around v to determine a maximum value (u_{max}) for the variable u of the integral; determining if the value for u_{max} is less than C, is between C and 1 or is more than 1; assigning the value of C to the variable v if u_{max} is less than C; assigning the value f u_{max} to the variable v if u_{max} is between C and 1; assigning the value of 1 to the variable v if u_{max} is more than 1; reducing the Taylor's series expansion of the Dirac coulombic tunnelling integral to an error function; reducing the error function to simple exponential functions by applying rational approximations to the error function; and calculating the enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the said simple exponential functions.

WO 00/77533 A2

Semiconductor Device Simulation Method and Simulator

The present invention relates to an automated simulation method for determining the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral and to a simulator for carrying out the method.

The enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device is considered to be responsible for a number of important effects in semiconductor devices, including the anomalous leakage current in polysilicon Thin Film Transistors (TFTs). Polysilicon TFTs are widely used for example in active matrix display devices. The anomalous leakage current of the TFTs can severely degrade the pixel voltage in such display devices. Thus, this is one example of the commercial importance of an automated simulation method and simulator of the type provided by the present invention.

Having regard to the complexity and cost of the fabrication processes for manufacturing semiconductor devices, it is highly desirable if not essential for the design and performance evaluation of such devices to be undertaken using mathematical simulations, often referred to as modelling. It is clearly crucial for such modelling to be able to provide accurate calculation of the enhanced generation-recombination rate due to trap-to-band tunnelling, and hence the leakage current, within a semiconductor device. Consequently, considerable effort has previously been spent in developing methods of calculating the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device. Such methods are embodied in computer programs which are sold as staple commercial products by or on behalf of their developers to designers and manufacturers of semiconductor devices.

In a paper submitted in 1996 and published in 1997 (Solid State Electronics Vol.41, No.4, pp 575-583 1997) the inventors hereof presented a generation-recombination model for device simulation including the Poole-Frenkel effect and phonon-assisted tunnelling. The model is conveniently referred to as the Dirac Coulombic Tunnelling Integral, which is recited as equation 1 in figure 9 hereof.

As noted in the above mentioned published paper, the Dirac Coulombic Tunnelling Integral is applicable to semiconductor devices generally. However, as also noted above, an important category of semiconductor devices is thin film transistors (TFTs) and such a device will herein after be used for ease of reference, but by way of one example only of a semiconductor device. Similarly, for ease of reference, the leakage current in a TFT will be referred to herein as a non-limiting example of the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device.

Figure 1 hereof is a graph showing voltage current characteristics of a polysilicon TFT. As seen in Fig. 1 when V_{DS} is high (5.1V), the leakage current (I_{DS}) increases with decreasing V_{GS} (below 0V). The magnitude of this leakage current poses as a significant problem, for example, when the TFT is employed as a switching pixel transistor in active matrix LCDs. Several field-assisted generation mechanisms have been proposed to explain this 'off' current.

A quantitative analysis of the leakage current in polysilicon TFTs based on the combination of current-voltage measurements as a function of temperature and 2-D simulations was carried out as long ago as 1995. This analysis shows that the dominant generation mechanism is pure trap-to-band tunnelling below 240K and phonon-assisted trap-to-band tunnelling at higher temperatures. The need to include Poole-Frenkel (PF) barrier lowering in trap-to-band phonon-assisted tunnelling was demonstrated for polysilicon pn junctions as long ago as 1982. Apart from further enhancing the emission rate for trap-to-band phonon-assisted tunnelling, the PF effect also plays a significant role in enhancing pure thermal emissions at low fields.

The PF effect consists of the lowering of a coulombic potential barrier due to the electric field applied to a semiconductor. For a trap to experience the effect, it must be neutral when filled (charged when empty). Such a trap potential is long ranged and is often referred to as a coulombic well. A trap that is neutral when empty will not experience the effect because of the absence of the coulomb potential. Such a trap potential is short ranged and is known as a Dirac well. Without the PF effect, the calculated emission rate is at least one order of magnitude lower than what is needed to fit the experimental data in polysilicon

TFTs. By using a 2-D simulator, based on the known trap-to-band phonon-assisted tunnelling model (Hurkx *et al*) available since 1992, the inventors hereof were unable to simulate the leakage currents in polysilicon TFTs accurately. This is because the conventional model takes only into account Dirac wells and deliberately neglects the PF effect. Moreover, the many attempts at modelling of trap-to-band phonon-assisted tunnelling inclusive of the PF effect, which have been made since development of the original theory by Vincent *et al* in 1979, do not address a key problem: the implementation in a device simulator. The work by Vincent *et al* in 1979 gives evidence both theoretically and experimentally that the electric field in a junction has a large influence on the thermal emission rate of deep levels (mid-gap states). This influence can be quantitatively explained in a model of phonon-assisted tunnelling emission. Tunnelling is very sensitive to the barrier height and is therefore expected to be considerably affected by the PF barrier lowering.

As noted above, in 1996 the present inventors presented a new quantum mechanical tunnelling generation-recombination (G-R) model, conveniently referred to as the Dirac Coulombic Tunnelling Integral, which takes into full rigorous account the PF barrier lowering and is suitable for implementation in a device simulator. This G-R model is consistently formulated for the entire range of electric fields and temperatures. At high fields, the dominant mechanism is found to be trap-to-band phonon-assisted tunnelling inclusive of the PF effect; while at low fields, the model will reduce to that of the standard Shockley-Read-Hall (SRH) thermal G-R.

However, a practical implementation of the model into commercial device simulators has not until this invention been presented despite the length of time since presentation of the Dirac Coulombic Tunnelling Integral and despite the high commercial value of such a practical implementation.

According to a first aspect of the present invention there is provided an automated simulation method for determining enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral, comprising the steps of:

assigning the variable C to the ratio of the Poole-Frenkel barrier lowering energy (ΔE_{fp}) divided by the energy range for which tunnelling can occur (ΔE_n);

assigning the value (C+1)/2 to a variable v and performing a second order Taylor's series expansion of the Dirac coulombic tunnelling integral around v to determine a maximum value (u_{max}) for the variable u of the integral;

determining if the value for u_{max} is less than C, is between C and 1 or is more than 1;

assigning the value of C to the variable v if u_{max} is less than C;

assigning the value of u_{max} to the variable v if u_{max} is between C and 1;

assigning the value of 1 to the variable v if u_{max} is more than 1;

reducing the Taylor's series expansion of the Dirac coulombic tunnelling integral to an error function;

reducing the error function to simple exponential functions by applying rational approximations to the error function; and

calculating the enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the said simple exponential functions.

According to a second aspect of the present invention there is provided a simulator for determining enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral, comprising:

means storing a variable C having a value equal to the ratio of the Poole-Frenkel barrier lowering energy (ΔE_{fp}) divided by the energy range for which tunnelling can occur (ΔE_n);

means which assign the value (C+1)/2 to a variable v and perform a second order Taylor's series expansion of the Dirac coulombic tunnelling integral around v to determine a maximum value (u_{max}) for the variable u of the integral;

means which determine if the value for u_{max} is less than C, is between C and 1 or is more than 1;

means which assign the value of C to the variable v if u_{max} is less than C;

means which assign the value of u_{max} to the variable v if u_{max} is between C and 1;

means which assign the value of 1 to the variable v if u_{max} is more than 1;

means storing simple exponential functions derived from applying rational approximations to an error function obtained by reducing the Taylor's series expansion of the Dirac coulombic tunnelling integral; and

means which calculate the enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the said simple exponential functions.

Although possible in theory, even with the fastest computers available today, using numerical integration methods to solve the Dirac coulombic tunnelling integral for every trap level in every element in a finite element package will take so much computation time that such an approach can not be used for a commercial and practicable implementation. The present invention enables such a commercial and practicable implementation. Moreover, the present invention can provide high levels of accuracy in the automated modelling of the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device.

Embodiments of the present invention will now be described in more detail by way of example only and with reference to the accompanying drawings, in which:

Figure 1 is a graph illustrating leakage current in a TFT;

Figure 2 shows two graphs illustrating a low field condition;

Figure 3 shows two graphs illustrating a moderate field condition;

Figure 4 shows two graphs illustrating a high field condition;

Figure 5 is a graph illustrating the performance of the present invention;

Figure 6 is a graph illustrating the performance of the present invention;

Figure 7 is a graph illustrating the performance of the present invention;

Figure 8 is a graph illustrating the performance of the present invention; and

Figure 9 lists equations useful in explaining embodiments of the present invention.

Starting from the Dirac coulombic tunnelling integral, given as Eqn.(1) in figure 9, it is possible for the integral to be expressed in the form shown as Eqn.(2). Applying the simplification shown in Eqn.(3) leads to Eqn.(4). Eqn.(4) can be further simplified to give Eqn.(5), where the function $f(u)$ is as defined in Eqn.(6).

Most of the contribution to the expression of Eqn.(5) can be expected to arise from the condition when the function $f(u)$ is largest. This condition should be considered for the three cases which have distinct characteristics namely, Case 1 when the electric field is low; Case 2 when the electric field is moderate and Case 3 when then the electric field is high. These three distinct conditions are illustrated in figures 2, 3 and 4 respectively.

Figure 2 is based on a low field value (F) of $F = 1x10^7 Vm^{-1}$ for $\Delta E_n = 0.5eV$. The maximum of $f(u)$ occurs at C, giving the maximum contribution to *exp[f(u)]* at C as well.

Figure 3 is based on a moderate field value (F) of $F = 7x10^7 Vm^{-1}$ for $\Delta E_n = 0.5eV$. The maximum of $f(u)$ occurs between C and 1, giving the maximum contribution to *exp[f(u)]* between C and 1 as well.

Figure 4 is based on a high field value (F) of $F = 1x10^8 Vm^{-1}$ for $\Delta E_n = 0.5eV$. The maximum of $f(u)$ occurs at 1, giving the maximum contribution to *exp[f(u)]* at 1 as well.

In a practical implementation it is convenient to consider Case 2 first. That is to determine the u_{max} for maximum $f(u)$ between C and 1. If u_{max} is less than C, then the condition of Case 1 is met. If u_{max} is more than 1 then the condition of Case 3 is met. Using a Taylor's series expansion, $f(u)$ can be approximated by a second-order series expansion around v, where $v = (C+1)/2$ as a reasonable estimate of where u_{max} is likely to occur. Thus is derived Eqn.(7), assuming $f(v)$ is as set out in Eqn.(8) and $f'(v)$ and $f''(v)$ are as set out in Eqn.(9) and Eqn.(10) respectively. Further, this enables $f(u)$ to be rewritten as in Eqn.(11).

From Eqn.(11), $f(u)$ can be differentiated once and the expression equated to zero, to obtain a stationary point, thus following the Eqn.s(12) to obtain a value for u_{max}. If this value of u_{max} is less than C then Case 1 exists. Then it is permissible to set $v = C$ since that is where the maximum $f(u)$ occurs. Then a second order Taylor's series expansion is performed about $v = C$. All of the necessary equations have been established, so it is only necessary to set $v = C$ in the simulator when u_{max} is less than C, so as to obtain an approximate second order expansion of $f(u)$ about C.

If u_{max} is between C and 1, Case 2 exists. In this condition, it is only necessary to set $v = u_{max}$ in the simulator, so as to obtain an approximate second order expansion of $f(u)$ about u_{max}. Here, of course, $v = u_{max}$ is no longer assumed to be equal to $(C+1)/2$.

If u_{max} is more than 1, Case 3 exists. In this condition, it is only necessary to set $v = 1$ in the simulator, so as to obtain an approximate second order expansion of $f(u)$ about 1.

With the appropriate value of v determined, Eqn.(11) is simplified to lead to Eqn.(13), where *AI*, *AII* and *AIII* are as set out in Eqn.(14), Eqn.(15) and Eqn.(16) respectively.

Completing the square on Eqn.(13) leads to Eqn.(17) and substituting Eqn.(17) into Eqn.(5) gives Eqn.(18). Next a value for t is assigned according to Eqn.(19) and for t_l and t_u when $u = C$ and $u = 1$ according to Eqn.(20) and Eqn.(21) respectively. The value of *du* is as shown by Eqn.(22).

Substitution of Eqn.s(19-22) in to Eqn.(18) leads to Eqn.(23). However, Eqn.(24) is known and a rational approximation thereof gives the function *erf*(x) as set out in Eqn.(25) with the values of t, a_1, a_2, a_3, a_4, a_5 and p as shown.

From Eqn.(24) is finally derived the approximated tunnelling integral according to the method of this embodiment of the present invention and as shown in Eqn.(26), with the values for *AI*, *AII*, *AIII*, t_l, t_u, $f(v)$, $f'(v)$, $f''(v)$, A, B, C, and D as shown. The values of v noted above for Case1, 2 and 3 are also listed for Eqn.(26) as is u_{max} for $v = (C+1)/2$. Of course, u_{max} is solved first in order to determine which of Cases 1, 2 and 3 apply.

An additional term should be respectively added or subtracted in Eqn.(26), as shown in Eqn.(27), if $(t_u > 0 \ \& \ t_l < 0)$ or $(t_u < 0 \ \& \ t_l > 0)$.

The present invention enables a commercial and practicable implementation of an automated simulation method for determining enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral. Moreover, the present invention can provide high levels of accuracy in the automated modelling of the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor

device. The method can be implemented in a two-dimensional finite element package.

The present invention uses the characteristics of low, moderate and high field regions with a Taylor's series expansion and a reduction to one or more error functions. Rational approximations are applied to the error functions so as to provide reduction to simple exponential functions. The metod enables cancelling of higher order terms in the exponential functions which otherwise cause premature overflow errors. This enables a much wider range to be calculated, as shown in figure 5.

The method of the invention enables the easy application of proper integration limits so as to ensure a smoth transition between low, moderate and high fields. The effect of removing discontinuities between the low, moderate and high field regions by avoiding conventional simplifications of the integration limits is illustrated in figure 6.

Figure 7 illustrates actual results of an implemention of the present invention for an n-channel polysilicon TFT as compared with the standard SRH model (no field enhancement) and the 1992 model by Hurkx *et al.* It is also to be noted that the implementation of the present invention more accurately simultes the leakage current at low field values (see figure 8 at $V_{DS} = 0.1V$).

Claims

1. An automated simulation method for determining enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral, comprising the steps of:

assigning the variable C to the ratio of the Poole-Frenkel barrier lowering energy (ΔE_{fp}) divided by the energy range for which tunnelling can occur (ΔE_n);

assigning the value (C+1)/2 to a variable v and performing a second order Taylor's series expansion of the Dirac coulombic tunnelling integral around v to determine a maximum value (u_{max}) for the variable u of the integral;

determining if the value for u_{max} is less than C, is between C and 1 or is more than 1;

assigning the value of C to the variable v if u_{max} is less than C;

assigning the value of u_{max} to the variable v if u_{max} is between C and 1;

assigning the value of 1 to the variable v if u_{max} is more than 1;

reducing the Taylor's series expansion of the Dirac coulombic tunnelling integral to an error function;

reducing the error function to simple exponential functions by applying rational approximations to the error function; and

calculating the enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the said simple exponential functions.

2. An automated simulation method which determines enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the approximated tunnelling equation set out as equation 26 herein.

3. An automated simulation method which determines enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the approximated tunnelling equation set out as equation 27 herein.

4. A simulator as claimed in any one of claims 1 to 3 which determines the leakage current in a polysilicon Thin Film Transistor.

5. A simulator for determining enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral, comprising:

means storing a variable C having a value equal to the ratio of the Poole-Frenkel barrier lowering energy (ΔE_{fp}) divided by the energy range for which tunnelling can occur (ΔE_n);

means which assign the value (C+1)/2 to a variable v and perform a second order Taylor's series expansion of the Dirac coulombic tunnelling integral around v to determine a maximum value (u_{max}) for the variable u of the integral;

means which determine if the value for u_{max} is less than C, is between C and 1 or is more than 1;

means which assign the value of C to the variable v if u_{max} is less than C;

means which assign the value of u_{max} to the variable v if u_{max} is between C and 1;

means which assign the value of 1 to the variable v if u_{max} is more than 1;

means storing simple exponential functions derived from applying rational approximations to an error function obtained by reducing the Taylor's series expansion of the Dirac coulombic tunnelling integral; and

means which calculate the enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the said simple exponential functions.

6. A simulator which determines enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device comprising means which calculate the approximated tunnelling equation set out as equation 26 herein.

7. A simulator which determines enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device comprising means which calculate the approximated tunnelling equation set out as equation 27 herein.

8. A simulator as claimed in any one of claims 5 to 7 which determines the leakage current in a polysilicon Thin Film Transistor.

Fig.1.

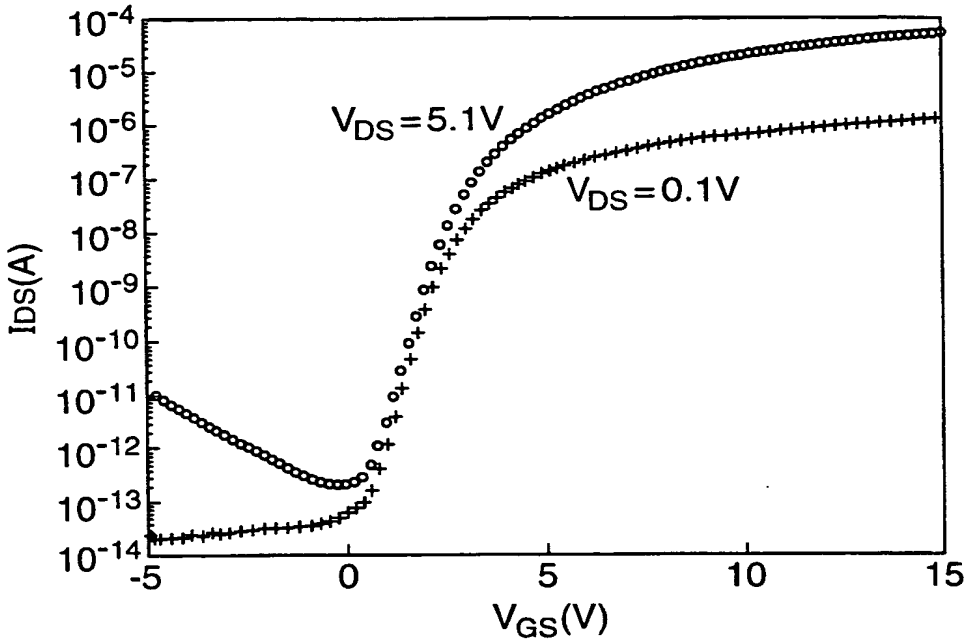
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
I_{DS}(A)
V_{DS}=5.1V
V_{DS}=0.1V
-5
0
5
10
15
V_{GS}(V)

Fig.5.

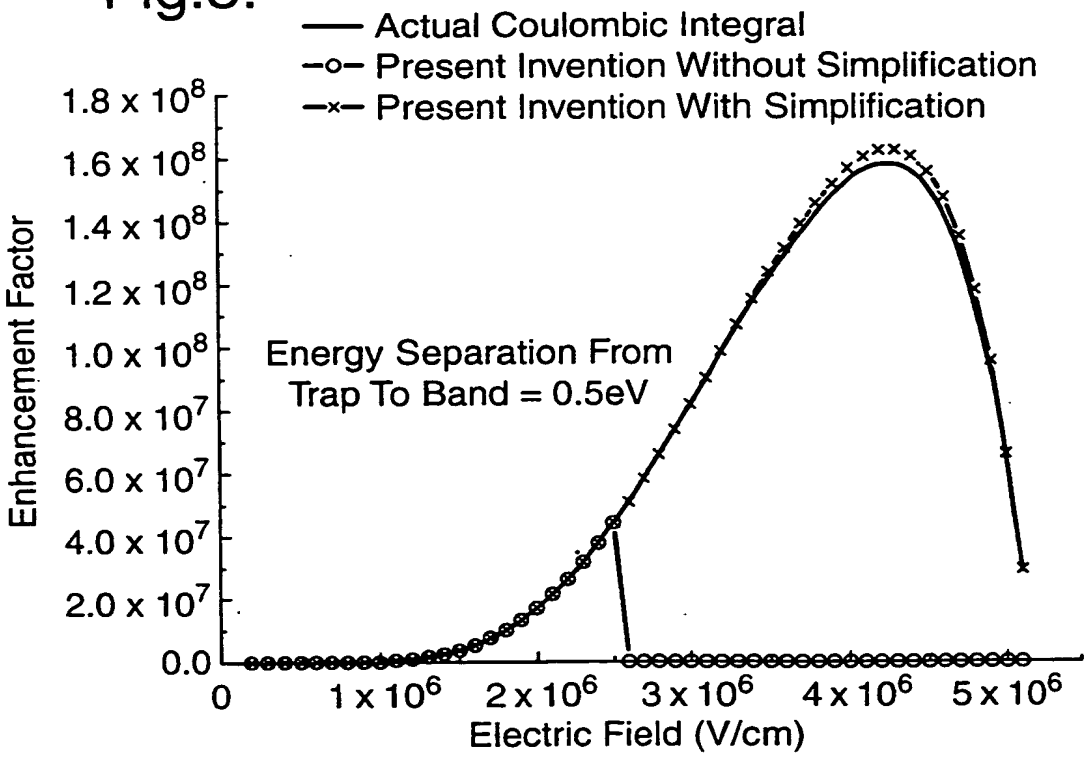
Actual Coulombic Integral
Present Invention Without Simplification
Present Invention With Simplification
1.8 x 10^8
1.6 x 10^8
1.4 x 10^8
1.2 x 10^8
1.0 x 10^8
8.0 x 10^7
6.0 x 10^7
4.0 x 10^7
2.0 x 10^7
0.0
Enhancement Factor
Energy Separation From
Trap To Band = 0.5eV
0
1 x 10^6
2 x 10^6
3 x 10^6
4 x 10^6
5 x 10^6
Electric Field (V/cm)

Fig.2.

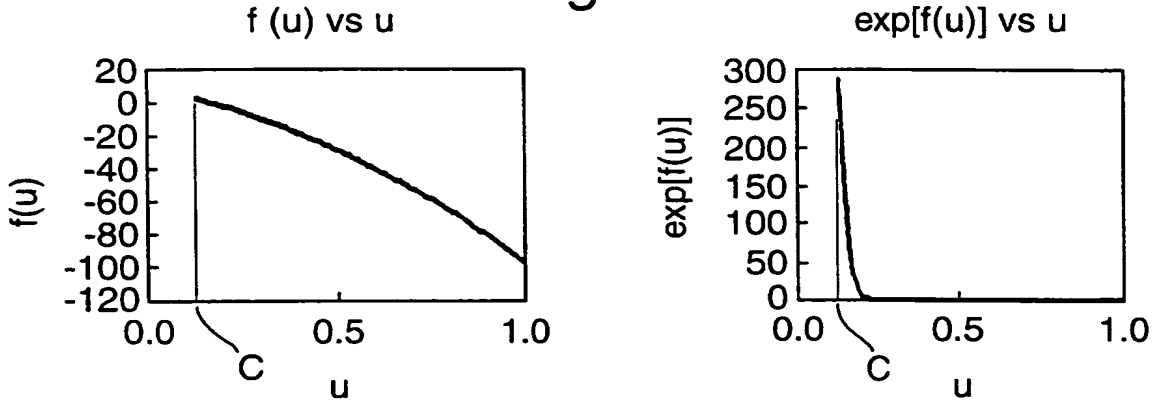

Fig.3.

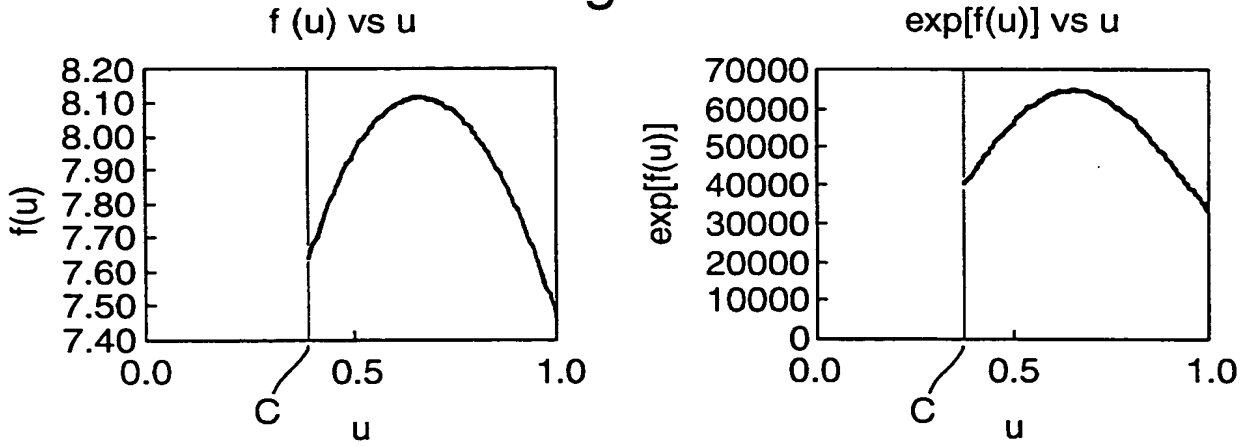

Fig.4.

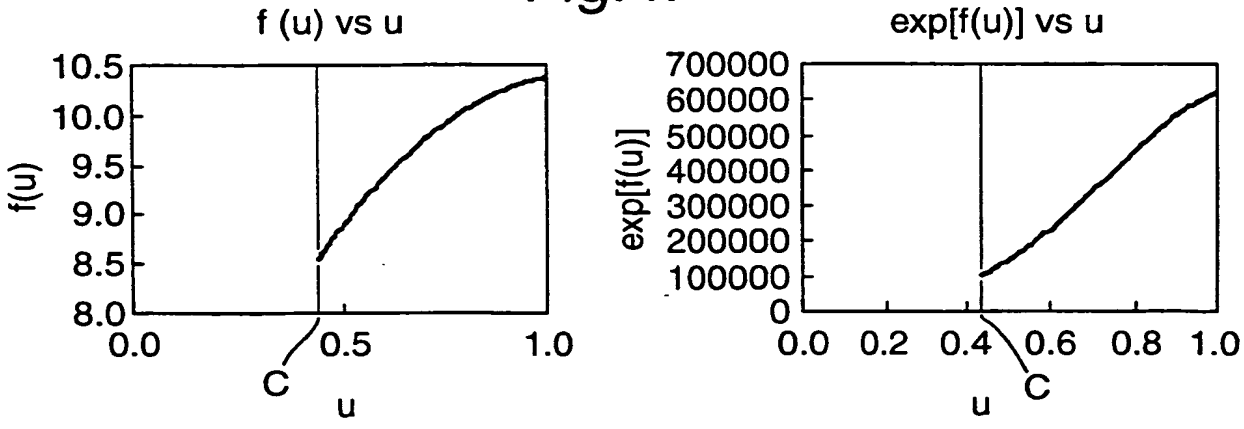

Fig.6.

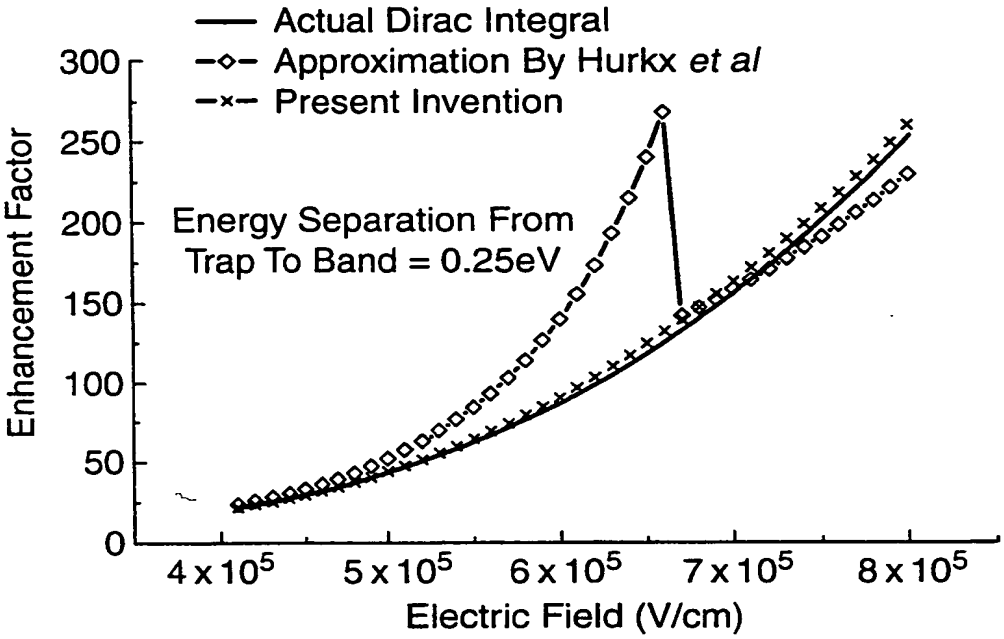
Actual Dirac Integral
Approximation By Hurkx et al
Present Invention
Energy Separation From
Trap To Band = 0.25eV
Enhancement Factor
300
250
200
150
100
50
0
4 x 10^5
5 x 10^5
6 x 10^5
7 x 10^5
8 x 10^5
Electric Field (V/cm)

Fig.7.

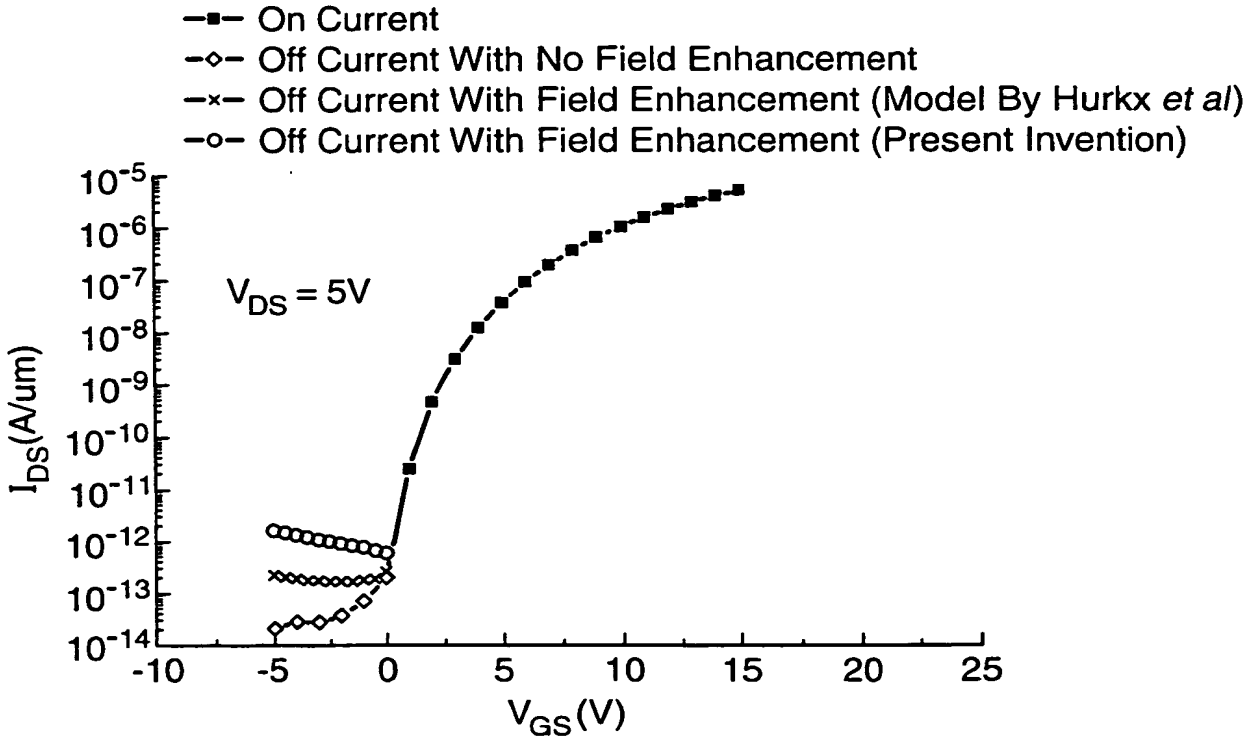
On Current
Off Current With No Field Enhancement
Off Current With Field Enhancement (Model By Hurkx et al)
Off Current With Field Enhancement (Present Invention)
V_DS = 5V
I_DS(A/um)
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
10^-11
10^-12
10^-13
10^-14
-10
-5
0
5
10
15
20
25
V_GS(V)

Fig.8.

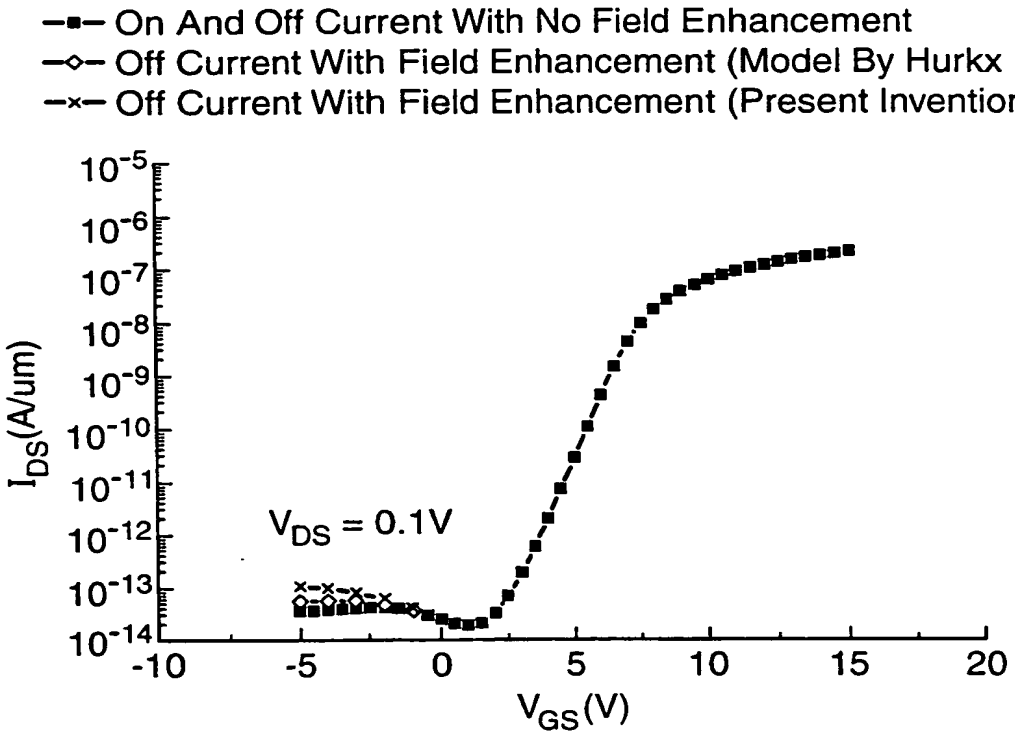
On And Off Current With No Field Enhancement
Off Current With Field Enhancement (Model By Hurkx et al)
Off Current With Field Enhancement (Present Invention)
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
I_{DS}(A/um)
V_{DS} = 0.1V
-10
-5
0
5
10
15
20
V_{GS}(V)

Fig.9.

$$\Gamma_n^{Coul} = \frac{\Delta E_n}{kT} \int_{\frac{\Delta E_{fp}}{\Delta E_n}}^{1} \exp\left\{ \frac{\Delta E_n}{kT} u - K_n u^{\frac{3}{2}} \left[1 - \left(\frac{\Delta E_{fp}}{u \Delta E_n} \right)^{\frac{5}{3}} \right] \right\} du \quad (1)$$

$$\Gamma_n^{Coul} = \frac{\Delta E_n}{kT} \int_{\frac{\Delta E_{fp}}{\Delta E_n}}^{1} \exp\left\{ \frac{\Delta E_n}{kT} u - K_n u^{\frac{3}{2}} + K_n \left(\frac{\Delta E_{fp}}{u \Delta E_n} \right)^{\frac{5}{3}} u^{-\frac{1}{6}} \right\} du. \quad (2)$$

$$A = \frac{\Delta E_n}{kT}, B = K_n, C = \frac{\Delta E_{fp}}{\Delta E_n}, D = BC^{\frac{5}{3}}. \quad (3)$$

$$\Gamma_n^{Coul} = A \int_c^1 \exp\left\{ Au - Bu^{\frac{3}{2}} + Du^{-\frac{1}{6}} \right\} du. \quad (4)$$

$$\Gamma_n^{Coul} = A \int_c^1 \exp\left[f(u) \right] du. \quad (5)$$

$$f(u) = Au - Bu^{\frac{3}{2}} + Du^{-\frac{1}{6}}. \quad (6)$$

$$f(u) \approx f(v) + f'(v)(u - v) + \frac{f''(v)}{2} (u - v)^2, \quad (7)$$

Fig.9(cont.a)

$$f(v) = Av - Bv^{\frac{3}{2}} + Dv^{-\frac{1}{6}}. \quad (8)$$

$$f'(v) = A - \frac{3}{2}Bv^{\frac{1}{2}} - \frac{1}{6}Dv^{-\frac{7}{6}}, \quad (9)$$

$$f''(v) = -\frac{3}{4}Bv^{-\frac{1}{2}} + \frac{7}{36}Dv^{-\frac{13}{6}}. \quad (10)$$

$$f(u) \approx \frac{f''(v)}{2}u^2 + [f'(v) - vf''(v)]u + \left[v^2\frac{f''(v)}{2} - vf'(v) + f(v)\right]. \quad (11)$$

$$f(u) \approx f''(v)\,u + [f'(v) - vf''(v)] = 0,$$

$$u_{max} = \frac{f'(v) - vf''(v)}{f''(v)}.$$

$$f(u) \approx -(AIu^2 + AIIu + AIII) \quad (12)$$

$$AI = -\frac{f''(v)}{2}. \quad (13)$$

$$AII = -[f'(v) - vf''(v)] \quad (14)$$

$$AIII = -\left[v^2\frac{f''(v)}{2} - vf'(v) + f(v)\right]. \quad (15)$$

$$f(u) \approx -AI\left[\left(u + \frac{AII}{2AI}\right)^2 + \left(\frac{AIII}{AI} - \left(\frac{AII}{2AI}\right)^2\right)\right]. \quad (16)$$

$$\Gamma_n^{Coul} = A\int_c^l \exp[f(u)]\,du \quad (17)$$

Fig.9(cont.b)

$$\Gamma_n^{Coul} = A \exp - \left[AI \left(\frac{AIII}{AI} - \left(\frac{AII}{2AI} \right)^2 \right) \right] \int_c^I \exp - \left[\sqrt{AI} \left(u + \frac{AII}{2AI} \right) \right]^2 du. \quad (18)$$

$$t = \sqrt{AI} \left(u + \frac{AII}{2AI} \right), \quad (19)$$

$$u = C,\ t_l = \sqrt{AI} \left(C + \frac{AII}{2AI} \right), \quad (20)$$

$$u = I,\ t_u = \sqrt{AI} \left(1 + \frac{AII}{2AI} \right), \quad (21)$$

$$du = \frac{1}{\sqrt{AI}}\, dt. \quad (22)$$

$$\Gamma_n^{Coul} = \frac{A}{\sqrt{AI}} \exp - \left[AI \left(\frac{AIII}{AI} - \left(\frac{AII}{2AI} \right)^2 \right) \right] \int_{t_l}^{t_u} e^{-t^2}\, dt. \quad (23)$$

$$\int_{t_l}^{t_u} e^{-t^2}\, dt = \frac{\sqrt{\pi}}{2} [erf(t_u) - erf(t_l)]. \quad (24)$$

$$erf(x) = 1 - (a_1 t + a_2 t^2 + a_3 t^3 + a_4 t^4 + a_5 t^5) e^{-x^2},$$

$$t = \frac{1}{1 + px},$$

$a_1 = 0.254829592;$
$a_2 = -0.284496736;$
$a_3 = 1.421413741;$
$a_4 = -1.453152027;$
$a_5 = 1.061405429;$
$p = 0.3275911;$ (25)

Fig.9(cont.c)

$$\Gamma_n^{Coul} = \frac{A}{2}\sqrt{\frac{\pi}{AI}}\left(\frac{a_1}{(1+pt_l)}+\frac{a_2}{(1+pt_l)^2}+\frac{a_3}{(1+pt_l)^3}+\frac{a_4}{(1+pt_l)^4}+\frac{a_5}{(1+pt_l)^5}\right)exp(-C^2AI - CAII - AIII)$$
$$- \frac{A}{2}\sqrt{\frac{\pi}{AI}}\left(\frac{a_1}{(1+pt_u)}+\frac{a_2}{(1+pt_u)^2}+\frac{a_3}{(1+pt_u)^3}+\frac{a_4}{(1+pt_u)^4}+\frac{a_5}{(1+pt_u)^5}\right)exp(-AI - AII - AIII) \quad (26)$$

$$AI = -\frac{f''(v)}{2},\ AII = -[f'(v) - vf''(v)],\ AIII = -\left[v^2\frac{f''(v)}{2} - vf'(v) + f(v)\right],$$

$$t_l = \sqrt{AI}\left(C+\frac{AII}{2AI}\right),\ t_u = \sqrt{AI}\left(1+\frac{AII}{2AI}\right),$$

$$f(v) = Av - Bv^{\frac{3}{2}} + Dv^{-\frac{1}{6}},$$

$$f'(v) = A - \frac{3}{2}Bv^{\frac{1}{2}} - \frac{1}{6}Dv^{-\frac{7}{6}},$$

$$f''(v) = -\frac{3}{4}Bv^{-\frac{1}{2}} + \frac{7}{36}Dv^{-\frac{13}{6}},$$

Fig.9(cont.d)

$$A = \frac{\Delta E_n}{kT},\ B = K_n, C = \frac{\Delta E_{fp}}{\Delta E_n},\ D = BC^{\frac{5}{3}}.$$

$v = C$(for $u_{max} < C$, case 1),

$v = u_{max}$ (for $C < u_{max} < I$, case 2),

$v = I$(for $u_{max} \geq 1$, case 3),

$$u_{max} = \frac{f'(v) - vf''(v)}{f''(v)} \text{ for } v = \frac{C+1}{2}.$$

$$\Gamma_n^{Coul} = \frac{A}{2}\sqrt{\frac{\pi}{AI}}\left(\frac{a_1}{(1+pt_l)} + \frac{a_2}{(1+pt_l)^2} + \frac{a_3}{(1+pt_l)^3} + \frac{a_4}{(1+pt_l)^4} + \frac{a_5}{(1+pt_l)^5}\right)exp(-C^2AI - CAII - AIII)$$
$$- \frac{A}{2}\sqrt{\frac{\pi}{AI}}\left(\frac{a_1}{(1+pt_u)} + \frac{a_2}{(1+pt_u)^2} + \frac{a_3}{(1+pt_u)^3} + \frac{a_4}{(1+pt_u)^4} + \frac{a_5}{(1+pt_u)^5}\right)exp(-AI - AII - AIII) \quad (27)$$
$$\pm \frac{A}{2}\sqrt{\frac{\pi}{AI}}\ \exp\left(-AIII + \frac{AII^2}{4AI}\right)$$

09176589

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 December 2000 (21.12.2000)

PCT

(10) International Publication Number
WO 00/77533 A3

(51) International Patent Classification[7]: G06F 17/50

(21) International Application Number: PCT/GB00/02321

(22) International Filing Date: 15 June 2000 (15.06.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
9913915.6 15 June 1999 (15.06.1999) GB

(71) Applicant *(for all designated States except US)*: SEIKO EPSON CORPORATION [JP/JP]; 4-1, Nishishinjuku 2-chome, Shinjuku-ku, Tokyo 163-0811 (JP).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: LUI, Basil [GB/GB]; Epson Cambridge Laboratory, 8c Kings Parade, Cambridge CB2 1SJ (GB).

(74) Agent: STURT, Clifford, Mark; Miller Sturt Kenyon, 9 John Street, London WC1N 2ES (GB).

(81) Designated States *(national)*: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*

(88) Date of publication of the international search report:
26 April 2001

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SEMICONDUCTOR DEVICE SIMULATION METHOD AND SIMULATOR

(57) Abstract: An automated simulation method for determining the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral and to a simulator for carrying out the method are disclosed. The method and simulator are, for example, particularly useful in the modelling of characteristics such as leakage current in polysilicon TFTs, which leakage current can, for example, seriously degrade pixel voltage in active matrix display devices. The simulator embodies the method, which method comprises the steps of: assigning the variable C to the ratio of the Poole-Frenkel barrier lowering energy (ΔE_{fp}) divided by the energy range for which tunnelling can occur (ΔE_n); assigning the value (C+1)/2 to a variable v and performing a second order Taylor's series expansion of the Dirac coulombic tunnelling integral around v to determine a maximum value (u_{max}) for the variable u of the integral; determining if the value for u_{max} is less than C, is between C and 1 or is more than 1; assigning the value of C to the variable v if u_{max} is less than C; assigning the value f u_{max} to the variable v if u_{max} is between C and 1; assigning the value of 1 to the variable v if u_{max} is more than 1; reducing the Taylor's series expansion of the Dirac coulombic tunnelling integral to an error functi n; reducing the error function to simple exponential functions by applying rational approximations to the error function; and calculating the enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the said simple exponential functions.

WO 00/77533 A3

INTERNATIONAL SEARCH REPORT

Inter. .onal Application No
PCT/GB 00/02321

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F17/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	LUI O K B ET AL: "A new generation-recombination model for device simulation including the Poole-Frenkel effect and phonon-assisted tunnelling" SOLID STATE ELECTRONICS,GB,ELSEVIER SCIENCE PUBLISHERS, BARKING, vol. 41, no. 4, 1 April 1997 (1997-04-01), pages 575-583, XP004056839 ISSN: 0038-1101 cited in the application the whole document	1-8

☐ Further documents are listed in the continuation of box C.

☐ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 December 2000	28/12/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Guingale, A

Form PCT/ISA/210 (second sheet) (July 1992)